blocks are present in the semiconductor memory device of FIG. 5.--

REMARKS

By this Preliminary Amendment, the specification has been revised to correct typographical errors. Claims 1-11 are presented herewith. Favorable consideration and early allowance of the present application is earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

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Respectfully submitted,

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[00057] Hereinafter, a comparison of the structures of the semiconductor memory devices of FIGS. 5 and 6 will be described. The semiconductor memory device of FIG. 5 includes the memory array blocks 31 through 38 that are each divided into three memory[-] sub_blocks 31a through 38a, respectively. Each memory sub-block has a memory cell of 352 bits per word line. That is, a total of twenty-four memory sub-blocks are present in the semiconductor memory device of FIG. 5.